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CHAPTER 4 SOLUTIONS 9 effort should be about 4. This design has imbalanced delays and excessive efforts. The path effort is $F = 12 * 6 * 9 = 648$. The best number of stages is 4 or 5. One way to speed the circuit up is to add a buffer (two inverters) at the end. The gates should be resized to bear efforts of $f = 648^{1/5} = 3.65$ each.

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Weste & Harris, CMOS VLSI Design: A Circuits and Systems ...
8 SOLUTIONS 2.1 2.2 In (a), the transistor sees $V_{gs} = V_{DD}$ and $V_{ds} = V_{DS}$. The current is I_n (b), the bottom transistor sees $V_{gs} = V_{DD}$ and $V_{ds} = V_1$. The top transistor sees $V_{gs} = V_{DD} - V_1$ and $V_{ds} = V_{DS} - V_1$. The currents are Solving for V_1 , we find Substituting V_1 into the I_{DS2} equation and simplifying gives $I_{DS1} = I_{DS2}$.

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David Money Harris Associate Professor of Engineering at Harvey Mudd College in Claremont, CA, holds a Ph.D. from Stanford University and S.B. and M.Eng. degrees from MIT. His research interests include CMOS VLSI design, microprocessors, and computer arithmetic. He holds a dozen patents, is the author of three other books in the field of digital design and three hiking guidebooks, and has ...

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